EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	117	forward adj body adj bias	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:45
L2	65237	sram	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:45
L3	43	1 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:45
L4	202	rom near5 standby	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:45
L5	69	tang-stephen-h$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:46
L6	76	khellah-muhammad-m$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:46
L7	111	somasekhar-dinesh.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:46
L8	238	de-vivek-k$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:47
L9	62	tschanz-james-w$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/06/05 16:47

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:39:56

Inventor Name Search Result

Your Search was:

Last Name = TANG
First Name = STEPHEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
10987278	Not Issued	83	11/12/2004	Level shifter	TANG, STEPHEN
11066395	7031203	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
11111060	7199617	150	04/21/2005	LEVEL SHIFTER	TANG, STEPHEN
10014009	Not Issued	161	12/10/2001	BALANCING GATE-LEAKAGE CURRENT IN DIFFERENTIAL PAIR CIRCUITS	TANG, STEPHEN H.
10025047	6693332	150	12/19/2001	CURRENT REFERENCE APPARATUS	TANG, STEPHEN H.
10162929	6643199	150	06/04/2002	MEMORY WITH REDUCED SUB-THRESHOLD LEAKAGE CURRENT IN DYNAMIC BIT LINES OF READ PORTS	TANG, STEPHEN H.
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	TANG, STEPHEN H.
10330652	7200068	150	12/27/2002	MULTI-PORTED REGISTER FILES	TANG, STEPHEN H.
10334644	6710642	150	12/30/2002	BIAS GENERATION CIRCUIT	TANG, STEPHEN H.
10673283	Not Issued	161	09/30/2003	Local bias generator for adaptive forward body bias	TANG, STEPHEN H.
10689128	6975005	150	10/20/2003	CURRENT REFERENCE APPARATUS AND SYSTEMS	TANG, STEPHEN H.
10716755	7072205	150	11/19/2003	FLOATING-BODY DRAM	TANG, STEPHEN

				WITH TWO-PHASE WRITE	H.
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	TANG, STEPHEN H.
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TANG, STEPHEN H.
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	TANG, STEPHEN H.
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	TANG, STEPHEN H.
10747084	6870418	150	12/30/2003	TEMPERATURE AND/OR PROCESS INDEPENDENT CURRENT GENERATION CIRCUIT	TANG, STEPHEN H.
10749734	7123500	150	12/30/2003	1P1N 2T GAIN CELL	TANG, STEPHEN H.
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	TANG, STEPHEN H.
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	TANG, STEPHEN H.
10812894	Not Issued	121	03/31/2004	SRAM device having forward body bias control	TANG, STEPHEN H.
10879480	7098507	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	TANG, STEPHEN H.
10879486	Not Issued	41	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of a processor	TANG, STEPHEN H.
10880337	7102358	150	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	TANG, STEPHEN H.
10881001	7120072	150	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	TANG, STEPHEN H.
10942019	Not Issued	61	09/16/2004	Charge storage memory cell	TANG, STEPHEN H.
10953865	Not Issued	61	09/30/2004	System and method for applying within-die adaptive body bias	TANG, STEPHEN H.

10954537	7110278	150	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	TANG, STEPHEN H.
10954931	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	TANG, STEPHEN H.
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	TANG, STEPHEN H.
10956285	Not Issued	41	09/30/2004	Non volatile data storage through dielectric breakdown	TANG, STEPHEN H.
10956407	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	TANG, STEPHEN H.
10979605	7102951	150	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	TANG, STEPHEN H.
10982266	7106128	150	11/03/2004	PROCESSOR APPARATUS WITH BODY BIAS CIRCUITRY TO DELAY THERMAL THROTTLING	TANG, STEPHEN H.
11008666	Not Issued	90	02/22/2005	2-TRANSISTOR FLOATING-BODY DRAM	TANG, STEPHEN H.
11027476	Not Issued	41	12/28/2004	One time programmable memory	TANG, STEPHEN H.
11038134	7164307	150	01/21/2005	BIAS GENERATOR FOR BODY BIAS	TANG, STEPHEN H.
11038394	Not Issued	95	01/21/2005	BIAS GENERATOR FOR BODY BIAS	TANG, STEPHEN H.
11053786	Not Issued	41	02/09/2005	Non strobe sensing circuit	TANG, STEPHEN H.
11134450	Not Issued	93	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	TANG, STEPHEN H.
11151982	7230846	150	06/14/2005	PURGE-BASED FLOATING BODY MEMORY	TANG, STEPHEN H.
11158518	7167397	150	06/21/2005	APPARATUS AND METHOD FOR PROGRAMMING A MEMORY ARRAY	TANG, STEPHEN H.
11170504	Not Issued	98	06/29/2005	CAPACITOR STRUCTURE FOR A LOGIC PROCESS	TANG, STEPHEN H.
11239903	Not Issued	93	09/30/2005	DUAL GATE OXIDE ONE TIME PROGRAMMABLE (OTP) ANTIFUSE CELL	TANG, STEPHEN H.
11268098	Not	41	11/07/2005	Asymmetric memory cell	TANG, STEPHEN

	Issued				H.
11268430	Not Issued	41	11/07/2005	Memory cell without halo implant	TANG, STEPHEN H.
11289621	7057927	150	11/30/2005	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	TANG, STEPHEN H.
11295400	Not Issued	30	12/06/2005	Component reliability budgeting system	TANG, STEPHEN H.
11320789	Not Issued	41	12/30/2005	Method and apparatus to clamp SRAM supply voltage	TANG, STEPHEN H.

Search and Display More Records.

Search Another: Inventor **Last Name** tang **First Name** stephen Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:40:04

Inventor Name Search Result

Your Search was:

Last Name = TANG
First Name = STEPHEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11429490	Not Issued	30	05/04/2006	Floating-body dynamic random access memory and method of fabrication in tri-gate technology	TANG, STEPHEN H.
10732493	6950771	150	12/09/2003	CORRELATION OF ELECTRICAL TEST DATA WITH PHYSICAL DEFECT DATA	TANG, STEPHEN WING-HO

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: tang First Name: stephen Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:40:40

Inventor Name Search Result

Your Search was:

Last Name = KHELLAH
First Name = MUHAMMAD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	KHELLAH, MUHAMMAD
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	KHELLAH, MUHAMMAD
11066395	7031203	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
11648297	Not Issued	19	12/29/2006	Address hashing to help distribute accesses across portions of destructive read cache memory	KHELLAH, MUHAMMAD
11648490	Not Issued	19	12/28/2006	Memory cell bit valve loss detection and restoration	KHELLAH, MUHAMMAD
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	KHELLAH, MUHAMMAD M.
10305753	6909652	150	11/26/2002	SRAM BIT-LINE REDUCTION	KHELLAH, MUHAMMAD M.
10330652	7200068	150	12/27/2002	MULTI-PORTED REGISTER FILES	KHELLAH, MUHAMMAD M.
10334410	6784688	150	12/30/2002	SKEWED REPEATER BUS	KHELLAH, MUHAMMAD M.
10334456	6831871	150	12/30/2002	STABLE MEMORY CELL READ	KHELLAH, MUHAMMAD M.

10334746	Not Issued	41	12/31/2002	Method and apparatus for bus repeater tapering	KHELLAH, MUHAMMAD M.
10716755	7072205	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	KHELLAH, MUHAMMAD M.
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	KHELLAH, MUHAMMAD M.
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	KHELLAH, MUHAMMAD M.
10738220	6876571	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	KHELLAH, MUHAMMAD M.
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	KHELLAH, MUHAMMAD M.
10749734	7123500	150	12/30/2003	1P1N 2T GAIN CELL	KHELLAH, MUHAMMAD M.
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	KHELLAH, MUHAMMAD M.
10810093	6985380	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	KHELLAH, MUHAMMAD M.
10812894	Not Issued	121	03/31/2004	SRAM device having forward body bias control	KHELLAH, MUHAMMAD M.
10813084	6992603	150	03/31/2004	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	KHELLAH, MUHAMMAD M.
10879480	7098507	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	KHELLAH, MUHAMMAD M.
10880337	7102358	150	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	KHELLAH, MUHAMMAD M.
10880988	Not Issued	41	06/30/2004	Interconnect structure in integrated circuits	KHELLAH, MUHAMMAD M.
10881001	7120072	150	06/30/2004	TWO TRANSISTOR GAIN	KHELLAH,

				CELL, METHOD, AND SYSTEM	MUHAMMAD M.
10942019	Not Issued	61	09/16/2004	Charge storage memory cell	KHELLAH, MUHAMMAD M.
10947765	7183795	150	09/23/2004	MAJORITY VOTER APPARATUS, SYSTEMS, AND METHODS	KHELLAH, MUHAMMAD M.
10954537	7110278	150	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	KHELLAH, MUHAMMAD M.
10954931	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	KHELLAH, MUHAMMAD M.
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
10956285	Not Issued	41	09/30/2004	Non volatile data storage through dielectric breakdown	KHELLAH, MUHAMMAD M.
10956407	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	KHELLAH, MUHAMMAD M.
10979605	7102951	150	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	KHELLAH, MUHAMMAD M.
11001870	Not Issued	61	12/01/2004	Memory circuit	KHELLAH, MUHAMMAD M.
11008666	Not Issued	90	02/22/2005	2-TRANSISTOR FLOATING-BODY DRAM	KHELLAH, MUHAMMAD M.
11027476	Not Issued	41	12/28/2004	One time programmable memory	KHELLAH, MUHAMMAD M.
11053786	Not Issued	41	02/09/2005	Non strobe sensing circuit	KHELLAH, MUHAMMAD M.
11053788	Not Issued	95	02/09/2005	MAJORITY VOTER CIRCUIT DESIGN	KHELLAH, MUHAMMAD M.
11059174	Not Issued	30	02/16/2005	Representative majority voter for bus invert coding	KHELLAH, MUHAMMAD M.
11134450	Not Issued	93	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	KHELLAH, MUHAMMAD M.
11137905	Not Issued	41	05/25/2005	Memory with dynamically adjustable supply	KHELLAH, MUHAMMAD M.
11151982	7230846	150	06/14/2005	PURGE-BASED FLOATING BODY MEMORY	KHELLAH, MUHAMMAD M.
11158518	7167397	150	06/21/2005	APPARATUS AND METHOD FOR PROGRAMMING A	KHELLAH, MUHAMMAD M.

				MEMORY ARRAY	
11169106	Not Issued	95	06/27/2005	MEMORY CELL DRIVER CIRCUITS	KHELLAH, MUHAMMAD M.
11170504	Not Issued	98	06/29/2005	CAPACITOR STRUCTURE FOR A LOGIC PROCESS	KHELLAH, MUHAMMAD M.
11172078	Not Issued	161	06/29/2005	Memory circuit	KHELLAH, MUHAMMAD M.
11172742	Not Issued	71	06/30/2005	Operating an information storage cell array	KHELLAH, MUHAMMAD M.
11225912	7230842	150	09/13/2005	MEMORY CELL HAVING P-TYPE PASS DEVICE	KHELLAH, MUHAMMAD M.

Search and Display More Records.

Search Another: Inventor **Last Name** khellah **First Name** muhammad Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:40:45

Inventor Name Search Result

Your Search was:

Last Name = KHELLAH
First Name = MUHAMMAD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11239903	Not Issued	93	09/30/2005	DUAL GATE OXIDE ONE TIME PROGRAMMABLE (OTP) ANTIFUSE CELL	KHELLAH, MUHAMMAD M.
11268098	Not Issued	41	11/07/2005	Asymmetric memory cell	KHELLAH, MUHAMMAD M.
11268430	Not Issued	41	11/07/2005	Memory cell without halo implant	KHELLAH, MUHAMMAD M.
11289621	7057927	150	11/30/2005	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	KHELLAH, MUHAMMAD M.
11314236	7190286	150	12/22/2005	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	KHELLAH, MUHAMMAD M.
11320789	Not Issued	41	12/30/2005	Method and apparatus to clamp SRAM supply voltage	KHELLAH, MUHAMMAD M.
11428247	Not Issued	25	06/30/2006	LOW POWER SERIAL LINK BUS ARCHITECTURE	KHELLAH, MUHAMMAD M.
11429490	Not Issued	30	05/04/2006	Floating-body dynamic random access memory and method of fabrication in tri-gate technology	KHELLAH, MUHAMMAD M.
11527782	Not Issued	30	09/27/2006	Memory driver circuits with embedded level shifters	KHELLAH, MUHAMMAD M.
11648399	Not Issued	19	12/28/2006	Memory having bit line with resistor(s) between memory cells	KHELLAH, MUHAMMAD M.

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: khellah First Name: muhammad Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:41:17

Inventor Name Search Result

Your Search was:

Last Name = SOMASEKHAR
First Name = DINESH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08412183	Not Issued	161	03/28/1995	APPARATUS AND METHOD FOR A REDUCED POWER MEMORY DIFFERENTIAL VOLTAGE SENSE-AMPLIFIER	SOMASEKHAR, DINESH
08937832	6014041	150	09/26/1997	DIFFERENTIAL CURRENT SWITCH LOGIC GATE	SOMASEKHAR, DINESH
08997071	6002272	150	12/23/1997	TRI-RAIL DOMINO CIRCUIT	SOMASEKHAR, DINESH
09539933	6421289	150	03/31/2000	METHOD AND APPARATUS FOR CHARGE-TRANSFER PRE-SENSING	SOMASEKHAR, DINESH
09690513	6496402	150	10/17/2000	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
09690687	6421269	150	10/17/2000	LOW-LEAKAGE MOS PLANAR CAPACITORS FOR USE WITHIN DRAM STORAGE CELLS	SOMASEKHAR, DINESH
09733216	6459316	150	12/08/2000	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
09733482	6701339	150	12/08/2000	PIPELINED COMPRESSOR CIRCUIT	SOMASEKHAR, DINESH
09740104	6351156	150	12/18/2000	Noise reduction circuit	SOMASEKHAR, DINESH
09796072	6982589	150	02/28/2001	MULTI-STAGE MULTIPLEXER	SOMASEKHAR, DINESH
09823575	6608786	150	03/30/2001	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	SOMASEKHAR, DINESH
09873557	7080111	150	06/04/2001	FLOATING POINT MULTIPLY ACCUMULATOR	SOMASEKHAR, DINESH

09873721	6889241	150	06/04/2001	FLOATING POINT ADDER	SOMASEKHAR, DINESH
09941053	6567329	150	08/28/2001	MULTIPLE WORD-LINE ACCESSING AND ACCESSOR	SOMASEKHAR, DINESH
09966586	6757784	150	09/28/2001	HIDING REFRESH OF MEMORY AND REFRESH-HIDDEN MEMORY	SOMASEKHAR, DINESH
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	SOMASEKHAR, DINESH
10208130	6597223	150	07/30/2002	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
10241791	6707708	150	09/10/2002	STATIC RANDOM ACCESS MEMORY WITH SYMMETRIC LEAKAGE-COMPENSATED BIT LINE	SOMASEKHAR, DINESH
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	SOMASEKHAR, DINESH
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	SOMASEKHAR, DINESH
10300398	6721222	150	11/19/2002	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
10305753	6909652	150	11/26/2002	SRAM BIT-LINE REDUCTION	SOMASEKHAR, DINESH
10316728	6707755	150	12/11/2002	HIGH VOLTAGE DRIVER	SOMASEKHAR, DINESH
10324177	6879531	150	12/19/2002	REDUCED READ DELAY FOR SINGLE-ENDED SENSING	SOMASEKHAR, DINESH
10324178	6724649	150	12/19/2002	MEMORY CELL LEAKAGE REDUCTION	SOMASEKHAR, DINESH
10334456	6831871	150	12/30/2002	STABLE MEMORY CELL READ	SOMASEKHAR, DINESH
10461293	6801465	150	06/13/2003	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	SOMASEKHAR, DINESH
10691342	Not	161	10/21/2003	Hiding refresh of memory and	SOMASEKHAR,

	Issued			refresh-hidden memory	DINESH
10716755	7072205	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	SOMASEKHAR, DINESH
10721178	Not Issued	93	11/26/2003	SYSTOLIC MEMORY ARRAYS	SOMASEKHAR, DINESH
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	SOMASEKHAR, DINESH
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	SOMASEKHAR, DINESH
10738220	6876571	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	SOMASEKHAR, DINESH
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	SOMASEKHAR, DINESH
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	SOMASEKHAR, DINESH
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	SOMASEKHAR, DINESH
10749734	7123500	150	12/30/2003	1P1N 2T GAIN CELL	SOMASEKHAR, DINESH
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	SOMASEKHAR, DINESH
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	SOMASEKHAR, DINESH
10810093	6985380	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	SOMASEKHAR, DINESH
10812894	Not Issued	121	03/31/2004	SRAM device having forward body bias control	SOMASEKHAR, DINESH
10879480	7098507	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	SOMASEKHAR, DINESH

10880337	7102358	150	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	SOMASEKHAR, DINESH
10881001	7120072	150	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	SOMASEKHAR, DINESH
10942019	Not Issued	61	09/16/2004	Charge storage memory cell	SOMASEKHAR, DINESH
10947869	7109776	150	09/23/2004	GATING FOR DUAL EDGE-TRIGGERED CLOCKING	SOMASEKHAR, DINESH
10954537	7110278	150	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	SOMASEKHAR, DINESH
10954931	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	SOMASEKHAR, DINESH
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	SOMASEKHAR, DINESH
10956285	Not Issued	41	09/30/2004	Non volatile data storage through dielectric breakdown	SOMASEKHAR, DINESH

Search and Display More Records.

Search Another: Inventor **Last Name** somasekhar **First Name** dinesh Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:41:21

Inventor Name Search Result

Your Search was:

Last Name = SOMASEKHAR
First Name = DINESH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10956407	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	SOMASEKHAR, DINESH
10979605	7102951	150	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	SOMASEKHAR, DINESH
10987278	Not Issued	83	11/12/2004	Level shifter	SOMASEKHAR, DINESH
11001870	Not Issued	61	12/01/2004	Memory circuit	SOMASEKHAR, DINESH
11008666	Not Issued	90	02/22/2005	2-TRANSISTOR FLOATING-BODY DRAM	SOMASEKHAR, DINESH
11027476	Not Issued	41	12/28/2004	One time programmable memory	SOMASEKHAR, DINESH
11053786	Not Issued	41	02/09/2005	Non strobe sensing circuit	SOMASEKHAR, DINESH
11066395	7031203	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	SOMASEKHAR, DINESH
11111060	7199617	150	04/21/2005	LEVEL SHIFTER	SOMASEKHAR, DINESH
11134450	Not Issued	93	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	SOMASEKHAR, DINESH
11137905	Not Issued	41	05/25/2005	Memory with dynamically adjustable supply	SOMASEKHAR, DINESH
11151982	7230846	150	06/14/2005	PURGE-BASED FLOATING BODY MEMORY	SOMASEKHAR, DINESH
11158518	7167397	150	06/21/2005	APPARATUS AND METHOD FOR PROGRAMMING A MEMORY ARRAY	SOMASEKHAR, DINESH
11169106	Not	95	06/27/2005	MEMORY CELL DRIVER	SOMASEKHAR,

	Issued			CIRCUITS	DINESH
11170504	Not Issued	98	06/29/2005	CAPACITOR STRUCTURE FOR A LOGIC PROCESS	SOMASEKHAR, DINESH
11172078	Not Issued	161	06/29/2005	Memory circuit	SOMASEKHAR, DINESH
11172742	Not Issued	71	06/30/2005	Operating an information storage cell array	SOMASEKHAR, DINESH
11225912	7230842	150	09/13/2005	MEMORY CELL HAVING P-TYPE PASS DEVICE	SOMASEKHAR, DINESH
11239903	Not Issued	93	09/30/2005	DUAL GATE OXIDE ONE TIME PROGRAMMABLE (OTP) ANTIFUSE CELL	SOMASEKHAR, DINESH
11268098	Not Issued	41	11/07/2005	Asymmetric memory cell	SOMASEKHAR, DINESH
11268430	Not Issued	41	11/07/2005	Memory cell without halo implant	SOMASEKHAR, DINESH
11289621	7057927	150	11/30/2005	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	SOMASEKHAR, DINESH
11320789	Not Issued	41	12/30/2005	Method and apparatus to clamp SRAM supply voltage	SOMASEKHAR, DINESH
11429490	Not Issued	30	05/04/2006	Floating-body dynamic random access memory and method of fabrication in tri-gate technology	SOMASEKHAR, DINESH
11527782	Not Issued	30	09/27/2006	Memory driver circuits with embedded level shifters	SOMASEKHAR, DINESH
11528812	Not Issued	25	09/27/2006	Digital outphasing transmitter architecture	SOMASEKHAR, DINESH
11542007	Not Issued	30	09/29/2006	Memory cell supply voltage control based on error detection	SOMASEKHAR, DINESH
11641006	Not Issued	25	12/19/2006	Signal generating circuit	SOMASEKHAR, DINESH
11644348	Not Issued	19	12/22/2006	Inverter based return-to-zero (RZ)+Non-RZ (NRZ) signaling	SOMASEKHAR, DINESH
11648399	Not Issued	19	12/28/2006	Memory having bit line with resistor(s) between memory cells	SOMASEKHAR, DINESH
11648490	Not Issued	19	12/28/2006	Memory cell bit valve loss detection and restoration	SOMASEKHAR, DINESH
11731193	Not	19	03/30/2007	Increasing the surface area of a	SOMASEKHAR,

	Issued			memory cell capacitor	DINESH
11731233	Not Issued	17	03/30/2007	High density memory	SOMASEKHAR, DINESH

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** somasekhar **First Name** dinesh Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:41:21

Inventor Name Search Result

Your Search was:

Last Name = SOMASEKHAR
First Name = DINESH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10956407	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	SOMASEKHAR, DINESH
10979605	7102951	150	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	SOMASEKHAR, DINESH
10987278	Not Issued	83	11/12/2004	Level shifter	SOMASEKHAR, DINESH
11001870	Not Issued	61	12/01/2004	Memory circuit	SOMASEKHAR, DINESH
11008666	Not Issued	90	02/22/2005	2-TRANSISTOR FLOATING-BODY DRAM	SOMASEKHAR, DINESH
11027476	Not Issued	41	12/28/2004	One time programmable memory	SOMASEKHAR, DINESH
11053786	Not Issued	41	02/09/2005	Non strobe sensing circuit	SOMASEKHAR, DINESH
11066395	7031203	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	SOMASEKHAR, DINESH
11111060	7199617	150	04/21/2005	LEVEL SHIFTER	SOMASEKHAR, DINESH
11134450	Not Issued	93	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	SOMASEKHAR, DINESH
11137905	Not Issued	41	05/25/2005	Memory with dynamically adjustable supply	SOMASEKHAR, DINESH
11151982	7230846	150	06/14/2005	PURGE-BASED FLOATING BODY MEMORY	SOMASEKHAR, DINESH
11158518	7167397	150	06/21/2005	APPARATUS AND METHOD FOR PROGRAMMING A MEMORY ARRAY	SOMASEKHAR, DINESH
11169106	Not	95	06/27/2005	MEMORY CELL DRIVER	SOMASEKHAR,

	Issued			CIRCUITS	DINESH
11170504	Not Issued	98	06/29/2005	CAPACITOR STRUCTURE FOR A LOGIC PROCESS	SOMASEKHAR, DINESH
11172078	Not Issued	161	06/29/2005	Memory circuit	SOMASEKHAR, DINESH
11172742	Not Issued	71	06/30/2005	Operating an information storage cell array	SOMASEKHAR, DINESH
11225912	7230842	150	09/13/2005	MEMORY CELL HAVING P-TYPE PASS DEVICE	SOMASEKHAR, DINESH
11239903	Not Issued	93	09/30/2005	DUAL GATE OXIDE ONE TIME PROGRAMMABLE (OTP) ANTIFUSE CELL	SOMASEKHAR, DINESH
11268098	Not Issued	41	11/07/2005	Asymmetric memory cell	SOMASEKHAR, DINESH
11268430	Not Issued	41	11/07/2005	Memory cell without halo implant	SOMASEKHAR, DINESH
11289621	7057927	150	11/30/2005	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	SOMASEKHAR, DINESH
11320789	Not Issued	41	12/30/2005	Method and apparatus to clamp SRAM supply voltage	SOMASEKHAR, DINESH
11429490	Not Issued	30	05/04/2006	Floating-body dynamic random access memory and method of fabrication in tri-gate technology	SOMASEKHAR, DINESH
11527782	Not Issued	30	09/27/2006	Memory driver circuits with embedded level shifters	SOMASEKHAR, DINESH
11528812	Not Issued	25	09/27/2006	Digital outphasing transmitter architecture	SOMASEKHAR, DINESH
11542007	Not Issued	30	09/29/2006	Memory cell supply voltage control based on error detection	SOMASEKHAR, DINESH
11641006	Not Issued	25	12/19/2006	Signal generating circuit	SOMASEKHAR, DINESH
11644348	Not Issued	19	12/22/2006	Inverter based return-to-zero (RZ)+Non-RZ (NRZ) signaling	SOMASEKHAR, DINESH
11648399	Not Issued	19	12/28/2006	Memory having bit line with resistor(s) between memory cells	SOMASEKHAR, DINESH
11648490	Not Issued	19	12/28/2006	Memory cell bit valve loss detection and restoration	SOMASEKHAR, DINESH
11731193	Not	19	03/30/2007	Increasing the surface area of a	SOMASEKHAR,

	Issued			memory cell capacitor	DINESH
11731233	Not Issued	17	03/30/2007	High density memory	SOMASEKHAR, DINESH

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** somasekhar **First Name** dinesh Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:41:41

Inventor Name Search Result

Your Search was:

Last Name = DE
First Name = VIVEK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08997071	6002272	150	12/23/1997	TRI-RAIL DOMINO CIRCUIT	DE, VIVEK
09001449	5986473	150	12/31/1997	DIFFERENTIAL, MIXED SWING, TRISTATE DRIVER CIRCUIT FOR HIGH PERFORMANCE AND LOW POWER ON-CHIP INTERCONNECTS	DE, VIVEK
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	DE, VIVEK
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	DE, VIVEK
10330652	7200068	150	12/27/2002	MULTI-PORTED REGISTER FILES	DE, VIVEK
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	DE, VIVEK
10748298	7030676	150	12/31/2003	TIMING CIRCUIT FOR SEPARATE POSITIVE AND NEGATIVE EDGE PLACEMENT IN A SWITCHING DC-DC CONVERTER	DE, VIVEK
10919672	Not Issued	25	08/16/2004	Stepwise drivers for DC/DC converters	DE, VIVEK
10924482	Not Issued	61	08/23/2004	DC/DC converters using dynamically-adjusted variable-size switches	DE, VIVEK
10954464	Not	71	09/30/2004	CPU power delivery system	DE, VIVEK

	Issued				
10987278	Not Issued	83	11/12/2004	Level shifter	DE, VIVEK
11066395	7031203	150	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	DE, VIVEK
11111060	7199617	150	04/21/2005	LEVEL SHIFTER	DE, VIVEK
11167978	Not Issued	41	06/27/2005	Voltage regulation using digital voltage control	DE, VIVEK
11170559	Not Issued	93	06/28/2005	LOW-VOLTAGE, BUFFERED BANDGAP REFERENCE WITH SELECTABLE OUTPUT VOLTAGE	DE, VIVEK
11173065	Not Issued	61	06/30/2005	Multiphase transformer for a multiphase DC-DC converter	DE, VIVEK
11173760	Not Issued	25	06/30/2005	DC-DC converter switching transistor current measurement technique	DE, VIVEK
11323675	Not Issued	30	12/30/2005	Error-detection flip-flop	DE, VIVEK
11542007	Not Issued	30	09/29/2006	Memory cell supply voltage control based on error detection	DE, VIVEK
11613134	Not Issued	16	12/19/2006	LOGIC CIRCUITS USING CARBON NANOTUBE TRANSISTORS	DE, VIVEK
11648209	Not Issued	16	12/29/2006	Methods of forming carbon nanotube transistors for high speed circuit operation and structures formed thereby	DE, VIVEK
11648297	Not Issued	19	12/29/2006	Address hashing to help distribute accesses across portions of destructive read cache memory	DE, VIVEK
11648399	Not Issued	19	12/28/2006	Memory having bit line with resistor(s) between memory cells	DE, VIVEK
11648490	Not Issued	19	12/28/2006	Memory cell bit valve loss detection and restoration	DE, VIVEK
11731193	Not Issued	19	03/30/2007	Increasing the surface area of a memory cell capacitor	DE, VIVEK
09218723	6154045	150	12/22/1998	METHOD AND APPARATUS FOR REDUCING SIGNAL TRANSMISSION DELAY USING SKEWED GATES	DE, VIVEK K

09470275	6518833	150	12/22/1999	LOW VOLTAGE PVT INSENSITIVE MOSFET BASED VOLTAGE REFERENCE CIRCUIT	DE, VIVEK K.
09505212	Not Issued	161	02/16/2000	Forward body biased transistors with reduced temperature	DE, VIVEK K.
09527344	6492837	150	03/17/2000	DOMINO LOGIC WITH OUTPUT PREDISCHARGE	DE, VIVEK K.
09537971	6359802	150	03/28/2000	One-transistor and one-capacitor dram cell for logic process technology	DE, VIVEK K.
09540230	Not Issued	161	03/31/2000	Footless domino gate	DE, VIVEK K.
09607495	6518796	150	06/30/2000	DYNAMIC CMOS CIRCUITS WITH INDIVIDUALLY ADJUSTABLE NOISE IMMUNITY	DE, VIVEK K.
09608314	6429711	150	06/30/2000	STACK-BASED IMPULSE FLIP-FLOP WITH STACK NODE PRE-CHARGE AND STACK NODE PRE-DISCHARGE	DE, VIVEK K.
09608457	6552887	150	06/29/2000	VOLTAGE DEPENDENT CAPACITOR CONFIGURATION FOR HIGHER SOFT ERROR RATE TOLERANCE	DE, VIVEK K.
09672689	6683467	150	09/29/2000	METHOD AND APPARATUS FOR PROVIDING ROTATIONAL BURN-IN STRESS TESTING	DE, VIVEK K.
09672695	6459293	150	09/29/2000	MULTIPLE PARAMETER TESTING WITH IMPROVED SENSITIVITY	DE, VIVEK K.
09672696	6632686	150	09/29/2000	SILICON ON INSULATOR DEVICE DESIGN HAVING IMPROVED FLOATING BODY EFFECT	DE, VIVEK K.
09675579	6519176	150	09/29/2000	DUAL THRESHOLD SRAM CELL FOR SINGLE-ENDED SENSING	DE, VIVEK K.
09677698	6849909	150	09/28/2000	METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR	DE, VIVEK K.
09690687	6421269	150	10/17/2000	LOW-LEAKAGE MOS PLANAR CAPACITORS FOR USE	DE, VIVEK K.

				WITHIN DRAM STORAGE CELLS	
09707528	6744301	150	11/07/2000	SYSTEM USING BODY-BIASED SLEEP TRANSISTORS TO REDUCE LEAKAGE POWER WHILE MINIMIZING PERFORMANCE PENALITIES AND NOISE	DE, VIVEK K.
09727025	Not Issued	161	11/30/2000	Reference voltage translation circuit	DE, VIVEK K.
09727173	6346803	150	11/30/2000	Current reference	DE, VIVEK K.
09727176	6433624	150	11/30/2000	THRESHOLD VOLTAGE GENERATION CIRCUIT	DE, VIVEK K.
09731515	6486706	150	12/06/2000	DOMINO LOGIC WITH LOW-THRESHOLD NMOS PULL-UP	DE, VIVEK K.
09740104	6351156	150	12/18/2000	Noise reduction circuit	DE, VIVEK K.
09820067	6429726	150	03/27/2001	ROBUST FORWARD BODY BIAS GENERATION CIRCUIT WITH DIGITAL TRIMMING FOR DC POWER SUPPLY VARIATION	DE, VIVEK K.
09820579	6608513	150	03/28/2001	FLIP-FLOP CIRCUIT HAVING DUAL-EDGE TRIGGERED PULSE GENERATOR	DE, VIVEK K.
09821531	6469572	150	03/28/2001	FORWARD BODY BIAS GENERATION CIRCUITS BASED ON DIODE CLAMPS	DE, VIVEK K.
09823575	6608786	150	03/30/2001	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	DE, VIVEK K.

Search and Display More Records.

Search Another: Inventor **Last Name** de **First Name** vivek Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:41:58

Inventor Name Search Result

Your Search was:

Last Name = DE
First Name = VIVEK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09823633	6496040	150	03/30/2001	TRADING OFF GATE DELAY VERSUS LEAKAGE CURRENT USING DEVICE STACK EFFECT	DE, VIVEK K.
09846514	Not Issued	161	04/30/2001	CMOS bus pulsing	DE, VIVEK K.
09846604	6515513	150	04/30/2001	REDUCING LEAKAGE CURRENTS IN INTEGRATED CIRCUITS	DE, VIVEK K.
09855910	6445216	150	05/14/2001	SENSE AMPLIFIER HAVING REDUCED VT MISMATCH IN INPUT MATCHED DIFFERENTIAL PAIR	DE, VIVEK K.
09894464	6518817	150	06/28/2001	VOLTAGE BUFFER	DE, VIVEK K.
09894465	6763484	150	06/28/2001	BODY BIAS USING SCAN CHAINS	DE, VIVEK K.
09941053	6567329	150	08/28/2001	MULTIPLE WORD-LINE ACCESSING AND ACCESSOR	DE, VIVEK K.
09957996	6593799	150	09/21/2001	CIRCUIT INCLUDING FORWARD BODY BIAS FROM SUPPLY VOLTAGE AND GROUND NODES	DE, VIVEK K.
10008532	Not Issued	161	11/05/2001	PMOS/NMOS circuits	DE, VIVEK K.
10010046	6642765	150	12/06/2001	TRANSMISSION-GATE BASED FLIP-FLOP	DE, VIVEK K.
10024467	6794630	150	12/17/2001	METHOD AND APPARATUS FOR ADJUSTING THE THRESHOLD OF A CMOS RADIATION-MEASURING CIRCUIT	DE, VIVEK K.
10025047	6693332	150	12/19/2001	CURRENT REFERENCE	DE, VIVEK K.

				APPARATUS	
10040903	6545619	150	12/28/2001	SWITCHED CURRENT SOURCE	DE, VIVEK K.
10162929	6643199	150	06/04/2002	MEMORY WITH REDUCED SUB-THRESHOLD LEAKAGE CURRENT IN DYNAMIC BIT LINES OF READ PORTS	DE, VIVEK K.
10183586	6566914	150	06/26/2002	SENSE AMPLIFIER HAVING REDUCED VT MISMATCH IN INPUT MATCHED DIFFERENTIAL PAIR	DE, VIVEK K.
10230466	6825687	150	08/29/2002	SELECTIVE COOLING OF AN INTEGRATED CIRCUIT FOR MINIMIZING POWER LOSS	DE, VIVEK K.
10241791	6707708	150	09/10/2002	STATIC RANDOM ACCESS MEMORY WITH SYMMETRIC LEAKAGE-COMPENSATED BIT LINE	DE, VIVEK K.
10254346	7053449	150	09/24/2002	DOUBLE GATE TRANSISTOR FOR LOW POWER CIRCUITS	DE, VIVEK K.
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	DE, VIVEK K.
10277009	6653866	150	10/21/2002	DOMINO LOGIC WITH OUTPUT PREDISCHARGE	DE, VIVEK K.
10300398	6721222	150	11/19/2002	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	DE, VIVEK K.
10305753	6909652	150	11/26/2002	SRAM BIT-LINE REDUCTION	DE, VIVEK K.
10322934	6710627	150	12/18/2002	DYNAMIC CMOS CIRCUITS WITH INDIVIDUALLY ADJUSTABLE NOISE IMMUNITY	DE, VIVEK K.
10324177	6879531	150	12/19/2002	REDUCED READ DELAY FOR SINGLE-ENDED SENSING	DE, VIVEK K.
10324178	6724649	150	12/19/2002	MEMORY CELL LEAKAGE REDUCTION	DE, VIVEK K.
10328573	7120804	150	12/23/2002	METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION THROUGH DYNAMIC CONTROL OF SUPPLY VOLTAGE AND BODY BIAS INCLUDING MAINTAINING A	DE, VIVEK K.

				SUBSTANTIALLY CONSTANT OPERATING FREQUENCY	
10330544	6806739	150	12/30/2002	TIME-BORROWING N-ONLY CLOCKED CYCLE LATCH	DE, VIVEK K.
10334410	6784688	150	12/30/2002	SKEWED REPEATER BUS	DE, VIVEK K.
10334456	6831871	150	12/30/2002	STABLE MEMORY CELL READ	DE, VIVEK K.
10334644	6710642	150	12/30/2002	BIAS GENERATION CIRCUIT	DE, VIVEK K.
10334746	Not Issued	41	12/31/2002	Method and apparatus for bus repeater tapering	DE, VIVEK K.
10461293	6801465	150	06/13/2003	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	DE, VIVEK K.
10620829	Not Issued	41	07/16/2003	CMOS radiation-measuring circuit with a variable threshold	DE, VIVEK K.
10673283	Not Issued	161	09/30/2003	Local bias generator for adaptive forward body bias	DE, VIVEK K.
10689128	6975005	150	10/20/2003	CURRENT REFERENCE APPARATUS AND SYSTEMS	DE, VIVEK K.
10703562	7096433	150	11/10/2003	METHOD FOR POWER CONSUMPTION REDUCTION	DE, VIVEK K.
10716755	7072205	150	11/19/2003	FLOATING-BODY DRAM WITH TWO-PHASE WRITE	DE, VIVEK K.
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	DE, VIVEK K.
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	DE, VIVEK K.
10738220	6876571	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	DE, VIVEK K.
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	DE, VIVEK K.
10745029	7015741	150	12/23/2003	ADAPTIVE BODY BIAS FOR CLOCK SKEW COMPENSATION	DE, VIVEK K.
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	DE, VIVEK K.

10746759	7051295	150	12/23/2003	IC DESIGN PROCESS INCLUDING AUTOMATED REMOVAL OF BODY CONTACTS FROM MOSFET DEVICES	DE, VIVEK K.
10747084	6870418	150	12/30/2003	TEMPERATURE AND/OR PROCESS INDEPENDENT CURRENT GENERATION CIRCUIT	DE, VIVEK K.
10747805	7075180	150	12/29/2003	METHOD AND APPARATUS FOR APPLYING BODY BIAS TO INTEGRATED CIRCUIT DIE	DE, VIVEK K.
10749734	7123500	150	12/30/2003	1P1N 2T GAIN CELL	DE, VIVEK K.
10749928	7015720	150	12/29/2003	DRIVER CIRCUIT	DE, VIVEK K.
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	DE, VIVEK K.
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	DE, VIVEK K.

Search and Display More Records.

Search Another: Inventor **Last Name** de **First Name** vivek Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:42:03

Inventor Name Search Result

Your Search was:

Last Name = DE
First Name = VIVEK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10760591	7098766	150	01/21/2004	MAGNETIC MATERIAL FOR TRANSFORMERS AND/OR INDUCTORS	DE, VIVEK K.
10781241	Not Issued	161	02/17/2004	Insulated channel field effect transistor with an electric field terminal region	DE, VIVEK K.
10792262	6917237	150	03/02/2004	TEMPERATURE DEPENDENT REGULATION OF THRESHOLD VOLTAGE	DE, VIVEK K.
10810093	6985380	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	DE, VIVEK K.
10812894	Not Issued	121	03/31/2004	SRAM device having forward body bias control	DE, VIVEK K.
10813084	6992603	150	03/31/2004	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	DE, VIVEK K.
10813169	6995605	150	03/31/2004	RESONANCE SUPPRESSION CIRCUIT	DE, VIVEK K.
10873243	6970018	150	06/23/2004	CLOCKED CYCLE LATCH CIRCUIT	DE, VIVEK K.
10877939	Not Issued	93	06/25/2004	SYSTEMS, MULTIPHASE POWER CONVERTERS WITH DROOP-CONTROL CIRCUITRY AND METHODS	DE, VIVEK K.
10879480	7098507	150	06/30/2004	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATION IN TRI-GATE TECHNOLOGY	DE, VIVEK K.
10879486	Not Issued	41	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of	DE, VIVEK K.

				a processor	
10879512	Not Issued	30	06/29/2004	Communications receiver with digital counter	DE, VIVEK K.
10880337	7102358	150	06/29/2004	OVERVOLTAGE DETECTION APPARATUS, METHOD, AND SYSTEM	DE, VIVEK K.
10880988	Not Issued	41	06/30/2004	Interconnect structure in integrated circuits	DE, VIVEK K.
10881001	7120072	150	06/30/2004	TWO TRANSISTOR GAIN CELL, METHOD, AND SYSTEM	DE, VIVEK K.
10942019	Not Issued	61	09/16/2004	Charge storage memory cell	DE, VIVEK K.
10947765	7183795	150	09/23/2004	MAJORITY VOTER APPARATUS, SYSTEMS, AND METHODS	DE, VIVEK K.
10947869	7109776	150	09/23/2004	GATING FOR DUAL EDGE-TRIGGERED CLOCKING	DE, VIVEK K.
10953178	7199657	150	09/30/2004	AMPLIFICATION GAIN STAGES HAVING REPLICA STAGES FOR DC BIAS CONTROL	DE, VIVEK K.
10953199	Not Issued	93	09/28/2004	FREQUENCY MANAGEMENT APPARATUS, SYSTEMS, AND METHODS	DE, VIVEK K.
10953865	Not Issued	61	09/30/2004	System and method for applying within-die adaptive body bias	DE, VIVEK K.
10954256	Not Issued	41	09/29/2004	Control circuitry in stacked silicon	DE, VIVEK K.
10954537	7110278	150	09/29/2004	CROSSPOINT MEMORY ARRAY UTILIZING ONE TIME PROGRAMMABLE ANTIFUSE CELLS	DE, VIVEK K.
10954931	7061806	150	09/30/2004	FLOATING-BODY MEMORY CELL WRITE	DE, VIVEK K.
10955383	Not Issued	93	09/30/2004	POWER MANAGEMENT INTEGRATED CIRCUIT	DE, VIVEK K.
10955746	Not Issued	25	09/30/2004	CPU power delivery system	DE, VIVEK K.
10956192	Not Issued	93	09/30/2004	APPARATUS AND METHOD FOR MULTI-PHASE TRANSFORMERS	DE, VIVEK K.
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	DE, VIVEK K.

10956285	Not Issued	41	09/30/2004	Non volatile data storage through dielectric breakdown	DE, VIVEK K.
10956407	7075821	150	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	DE, VIVEK K.
10977145	7208963	150	10/29/2004	METHOD AND APPARATUS FOR MEASURING COIL CURRENT	DE, VIVEK K.
10979605	7102951	150	11/01/2004	OTP ANTIFUSE CELL AND CELL ARRAY	DE, VIVEK K.
10982266	7106128	150	11/03/2004	PROCESSOR APPARATUS WITH BODY BIAS CIRCUITRY TO DELAY THERMAL THROTTLING	DE, VIVEK K.
11001870	Not Issued	61	12/01/2004	Memory circuit	DE, VIVEK K.
11008666	Not Issued	90	02/22/2005	2-TRANSISTOR FLOATING-BODY DRAM	DE, VIVEK K.
11018011	Not Issued	161	12/20/2004	Body biasing for dynamic circuit	DE, VIVEK K.
11018016	Not Issued	41	12/20/2004	Body biasing methods and circuits	DE, VIVEK K.
11027476	Not Issued	41	12/28/2004	One time programmable memory	DE, VIVEK K.
11027696	Not Issued	90	12/28/2004	LEAKAGE CURRENT MANAGEMENT	DE, VIVEK K.
11038134	7164307	150	01/21/2005	BIAS GENERATOR FOR BODY BIAS	DE, VIVEK K.
11038394	Not Issued	95	01/21/2005	BIAS GENERATOR FOR BODY BIAS	DE, VIVEK K.
11053786	Not Issued	41	02/09/2005	Non strobe sensing circuit	DE, VIVEK K.
11053788	Not Issued	95	02/09/2005	MAJORITY VOTER CIRCUIT DESIGN	DE, VIVEK K.
11059174	Not Issued	30	02/16/2005	Representative majority voter for bus invert coding	DE, VIVEK K.
11094574	Not Issued	61	03/31/2005	Method and apparatus to adjust die frequency	DE, VIVEK K.
11095951	Not Issued	71	03/31/2005	Signal measurement systems and methods	DE, VIVEK K.
11134450	Not Issued	93	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	DE, VIVEK K.

11137905	Not Issued	41	05/25/2005	Memory with dynamically adjustable supply	DE, VIVEK K.
11151982	7230846	150	06/14/2005	PURGE-BASED FLOATING BODY MEMORY	DE, VIVEK K.
11158518	7167397	150	06/21/2005	APPARATUS AND METHOD FOR PROGRAMMING A MEMORY ARRAY	DE, VIVEK K.

Search and Display More Records.

Search Another: Inventor **Last Name** de **First Name** vivek Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:42:10

Inventor Name Search Result

Your Search was:

Last Name = DE
First Name = VIVEK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11169106	Not Issued	95	06/27/2005	MEMORY CELL DRIVER CIRCUITS	DE, VIVEK K.
11170504	Not Issued	98	06/29/2005	CAPACITOR STRUCTURE FOR A LOGIC PROCESS	DE, VIVEK K.
11172078	Not Issued	161	06/29/2005	Memory circuit	DE, VIVEK K.
11172250	Not Issued	25	06/30/2005	0th droop detector architecture and implementation	DE, VIVEK K.
11172742	Not Issued	71	06/30/2005	Operating an information storage cell array	DE, VIVEK K.
11194946	Not Issued	41	08/01/2005	Leakage current reduction scheme for domino circuits	DE, VIVEK K.
11225912	7230842	150	09/13/2005	MEMORY CELL HAVING P-TYPE PASS DEVICE	DE, VIVEK K.
11239903	Not Issued	93	09/30/2005	DUAL GATE OXIDE ONE TIME PROGRAMMABLE (OTP) ANTIFUSE CELL	DE, VIVEK K.
11268098	Not Issued	41	11/07/2005	Asymmetric memory cell	DE, VIVEK K.
11268430	Not Issued	41	11/07/2005	Memory cell without halo implant	DE, VIVEK K.
11277117	Not Issued	41	03/21/2006	DRIVER CIRCUIT	DE, VIVEK K.
11289621	7057927	150	11/30/2005	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	DE, VIVEK K.
11295400	Not Issued	30	12/06/2005	Component reliability budgeting system	DE, VIVEK K.
11314236	7190286	150	12/22/2005	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	DE, VIVEK K.

11320789	Not Issued	41	12/30/2005	Method and apparatus to clamp SRAM supply voltage	DE, VIVEK K.
11321100	Not Issued	25	12/29/2005	Reliability degradation compensation using body bias	DE, VIVEK K.
11323369	Not Issued	30	12/29/2005	Statistical circuit design with carbon nanotubes	DE, VIVEK K.
11324628	Not Issued	25	01/03/2006	Bidirectional body bias regulation	DE, VIVEK K.
11428247	Not Issued	25	06/30/2006	LOW POWER SERIAL LINK BUS ARCHITECTURE	DE, VIVEK K.
11429490	Not Issued	30	05/04/2006	Floating-body dynamic random access memory and method of fabrication in tri-gate technology	DE, VIVEK K.
11486030	Not Issued	30	07/14/2006	Method and apparatus for power consumption reduction	DE, VIVEK K.
11527782	Not Issued	30	09/27/2006	Memory driver circuits with embedded level shifters	DE, VIVEK K.
08795652	5841299	150	02/06/1997	METHOD AND APPARATUS FOR IMPLEMENTING AN ADIABATIC LOGIC FAMILY	DE, VIVEK K.
08880047	6166584	150	06/20/1997	FOWARD BIASED MOS CIRCUITS	DE, VIVEK K.
08908582	5986476	150	08/08/1997	METHOD AND APPARATUS FOR IMPLEMENTING A DYNAMIC ADIABATIC LOGIC FAMILY	DE, VIVEK K.
09078388	6232827	150	05/13/1998	TRANSISTORS PROVIDING DESIRED THRESHOLD VOLTAGE AND REDUCED SHORT CHANNEL EFFECTS WITH FORWARD BODY BIAS	DE, VIVEK K.
09078395	6300819	150	05/13/1998	CIRCUIT INCLUDING FORWARD BODY BIAS FROM SUPPLY VOLTAGE AND GROUND NODES	DE, VIVEK K.
09078424	6218895	150	05/13/1998	MULTIPLE WELL TRANSISTOR CIRCUITS HAVING FORWARD BODY BIAS	DE, VIVEK K.
09078432	6100751	150	05/13/1998	FORWARD BODY BIASED FIELD EFFECT TRANSISTOR PROVIDING DECOUPLING CAPACITANCE	DE, VIVEK K.
09150869	6191606	150	09/10/1998	METHOD AND APPARATUS FOR REDUCING STANDBY	DE, VIVEK K.

				LEAKAGE CURRENT USING INPUT VECTOR ACTIVATION	
09151177	6169419	150	09/10/1998	METHOD AND APPARATUS FOR REDUCING STANDBY LEAKAGE CURRENT USING A TRANSISTOR STACK EFFECT	DE, VIVEK K.
09151827	6329874	150	09/11/1998	METHOD AND APPARATUS FOR REDUCING STANDBY LEAKAGE CURRENT USING A LEAKAGE CONTROL TRANSISTOR THAT RECEIVES BOOSTED GATE DRIVE DURING AN ACTIVE MODE	DE, VIVEK K.
09165483	6734498	150	10/02/1998	INSULATED CHANNEL FIELD EFFECT TRANSISTOR WITH AN ELECTRIC FIELD TERMINAL REGION	DE, VIVEK K.
09224573	6484265	150	12/30/1998	SOFTWARE CONTROL OF TRANSISTOR BODY BIAS IN CONTROLLING CHIP PARAMETERS	DE, VIVEK K.
09224574	6272666	150	12/30/1998	TRANSISTOR GROUP MISMATCH DETECTION AND REDUCTION	DE, VIVEK K.
09224575	6411156	150	12/30/1998	EMPLOYING TRANSISTOR BODY BIAS IN CONTROLLING CHIP PARAMETERS	DE, VIVEK K.
09256842	6218892	150	02/24/1999	DIFFERENTIAL CIRCUITS EMPLOYING FORWARD BODY BIAS	DE, VIVEK K.
09261915	6181608	150	03/03/1999	DUAL VT SRAM CELL WITH BITLINE LEAKAGE CONTROL	DE, VIVEK K.
09406938	6529045	150	09/28/1999	NMOS PRECHARGE DOMINO LOGIC	DE, VIVEK K.
09451661	6366156	150	11/30/1999	FORWARD BODY BIAS VOLTAGE GENERATION SYSTEMS	DE, VIVEK K.
09452080	6448840	150	11/30/1999	ADAPTIVE BODY BIASING CIRCUIT AND METHOD	DE, VIVEK K.
09460742	Not Issued	161	12/14/1999	DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION	DE, VIVEK K.
09469406	6828638	150	12/22/1999	DECOUPLING CAPACITORS FOR THIN GATE OXIDES	DE, VIVEK K.

09470291	6177788	150	12/22/1999	NONLINEAR BODY EFFECT COMPENSATED MOSFET VOLTAGE REFERENCE	DE, VIVEK K.
09474533	6275071	150	12/29/1999	DOMINO LOGIC CIRCUIT AND METHOD	DE, VIVEK K.
09690513	6496402	150	10/17/2000	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	DE, VIVEK K.
60005791	Not Issued	159	10/23/1995	CAMOS: COMPLEMENTARY STATIC ADIABATIC LOGIC	DE, VIVEK K.
60009297	Not Issued	159	12/05/1995	ADMOS: STATIC ADIABATIC-REVERSIBLE LOGIC	DE, VIVEK K.
60009321	Not Issued	159	12/28/1995	REVERSIBLE ADIABATIC METAL-OXIDE-SEMICONDUCTOR (RAMOS) CIRCUITS: A NEW DYNAMIC REVERSIBLE ADIABATIC LOGIC FAMILY	DE, VIVEK K.
60009401	Not Issued	159	12/28/1995	DYNAMIC ADIABATIC METAL-OXIDE-SEMICONDUCTOR (DAMOS) CIRCUITS: A NEW DYNAMIC ENERGY-RECYCLING LOGIC FAMILY	DE, VIVEK K.

Search and Display More Records.

Search Another: Inventor **Last Name** de **First Name** vivek Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:42:15

Inventor Name Search Result

Your Search was:

Last Name = DE
First Name = VIVEK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09672340	6300812	150	09/28/2000	Process, voltage,and temperature insensitive two phase clock generation circuit	DE., VIVEK K.
06879489	4831023	150	06/27/1986	WATER WASHABLE VEHICLES FOR TOPICAL USE	DESAI, VIVEK
09621623	6656505	150	07/21/2000	METHOD FOR FORMING AN AQUEOUS FLOCCULATED SUSPENSION	DESAI, VIVEK
09707793	Not Issued	161	11/08/2000	Flocculated pharmaceutical suspensions and methods for actives	DESAI, VIVEK
10440200	Not Issued	161	05/19/2003	Flocculated pharmaceutical suspensions and methods for actives	DESAI, VIVEK
10628227	Not Issued	161	07/29/2003	Pharmaceutical suspensions, compositions and methods	DESAI, VIVEK
10828344	Not Issued	41	04/21/2004	Flocculated pharmaceutical suspensions and methods for actives	DESAI, VIVEK
60824222	Not Issued	20	08/31/2006	Automated Blood Draw System	DESHMUKH, VIVEK R.
60824234	Not Issued	20	08/31/2006	Inflatable Surgical Retractor	DESHMUKH, VIVEK R.
11169469	Not Issued	30	06/29/2005	Browser based remote control of functional testing tool	DEVAS, VIVEK

Inventor Search Completed: No Records to Display.

Search Another: Inventor Last Name: de First Name: vivek Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

PALM INTRANET

Day : Tuesday
Date: 6/5/2007
Time: 08:42:42

Inventor Name Search Result

Your Search was:

Last Name = TSCHANZ
First Name = JAMES

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10956195	7206249	150	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	TSCHANZ, JAMES
11323675	Not Issued	30	12/30/2005	Error-detection flip-flop	TSCHANZ, JAMES
09608314	6429711	150	06/30/2000	STACK-BASED IMPULSE FLIP-FLOP WITH STACK NODE PRE-CHARGE AND STACK NODE PRE-DISCHARGE	TSCHANZ, JAMES W.
09672696	6632686	150	09/29/2000	SILICON ON INSULATOR DEVICE DESIGN HAVING IMPROVED FLOATING BODY EFFECT	TSCHANZ, JAMES W.
09707528	6744301	150	11/07/2000	SYSTEM USING BODY-BIASED SLEEP TRANSISTORS TO REDUCE LEAKAGE POWER WHILE MINIMIZING PERFORMANCE PENALITIES AND NOISE	TSCHANZ, JAMES W.
09820579	6608513	150	03/28/2001	FLIP-FLOP CIRCUIT HAVING DUAL-EDGE TRIGGERED PULSE GENERATOR	TSCHANZ, JAMES W.
09846514	Not Issued	161	04/30/2001	CMOS bus pulsing	TSCHANZ, JAMES W.
09846604	6515513	150	04/30/2001	REDUCING LEAKAGE CURRENTS IN INTEGRATED CIRCUITS	TSCHANZ, JAMES W.
09894465	6763484	150	06/28/2001	BODY BIAS USING SCAN CHAINS	TSCHANZ, JAMES W.
10010046	6642765	150	12/06/2001	TRANSMISSION-GATE BASED FLIP-FLOP	TSCHANZ, JAMES W.
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	TSCHANZ, JAMES W.

10328573	7120804	150	12/23/2002	METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION THROUGH DYNAMIC CONTROL OF SUPPLY VOLTAGE AND BODY BIAS INCLUDING MAINTAINING A SUBSTANTIALLY CONSTANT OPERATING FREQUENCY	TSCHANZ, JAMES W.
10330544	6806739	150	12/30/2002	TIME-BORROWING N-ONLY CLOCKED CYCLE LATCH	TSCHANZ, JAMES W.
10334410	6784688	150	12/30/2002	SKEWED REPEATER BUS	TSCHANZ, JAMES W.
10334746	Not Issued	41	12/31/2002	Method and apparatus for bus repeater tapering	TSCHANZ, JAMES W.
10673283	Not Issued	161	09/30/2003	Local bias generator for adaptive forward body bias	TSCHANZ, JAMES W.
10703562	7096433	150	11/10/2003	METHOD FOR POWER CONSUMPTION REDUCTION	TSCHANZ, JAMES W.
10738216	7020041	150	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TSCHANZ, JAMES W.
10745029	7015741	150	12/23/2003	ADAPTIVE BODY BIAS FOR CLOCK SKEW COMPENSATION	TSCHANZ, JAMES W.
10746759	7051295	150	12/23/2003	IC DESIGN PROCESS INCLUDING AUTOMATED REMOVAL OF BODY CONTACTS FROM MOSFET DEVICES	TSCHANZ, JAMES W.
10747805	7075180	150	12/29/2003	METHOD AND APPARATUS FOR APPLYING BODY BIAS TO INTEGRATED CIRCUIT DIE	TSCHANZ, JAMES W.
10792262	6917237	150	03/02/2004	TEMPERATURE DEPENDENT REGULATION OF THRESHOLD VOLTAGE	TSCHANZ, JAMES W.
10812894	Not Issued	121	03/31/2004	SRAM device having forward body bias control	TSCHANZ, JAMES W.
10813084	6992603	150	03/31/2004	SINGLE-STAGE AND MULTI-STAGE LOW POWER INTERCONNECT ARCHITECTURES	TSCHANZ, JAMES W.
10873243	6970018	150	06/23/2004	CLOCKED CYCLE LATCH CIRCUIT	TSCHANZ, JAMES W.

10879486	Not Issued	41	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of a processor	TSCHANZ, JAMES W.
10880988	Not Issued	41	06/30/2004	Interconnect structure in integrated circuits	TSCHANZ, JAMES W.
10947765	7183795	150	09/23/2004	MAJORITY VOTER APPARATUS, SYSTEMS, AND METHODS	TSCHANZ, JAMES W.
10947869	7109776	150	09/23/2004	GATING FOR DUAL EDGE-TRIGGERED CLOCKING	TSCHANZ, JAMES W.
10953199	Not Issued	93	09/28/2004	FREQUENCY MANAGEMENT APPARATUS, SYSTEMS, AND METHODS	TSCHANZ, JAMES W.
10953865	Not Issued	61	09/30/2004	System and method for applying within-die adaptive body bias	TSCHANZ, JAMES W.
10954256	Not Issued	41	09/29/2004	Control circuitry in stacked silicon	TSCHANZ, JAMES W.
10955383	Not Issued	93	09/30/2004	POWER MANAGEMENT INTEGRATED CIRCUIT	TSCHANZ, JAMES W.
10982266	7106128	150	11/03/2004	PROCESSOR APPARATUS WITH BODY BIAS CIRCUITRY TO DELAY THERMAL THROTTLING	TSCHANZ, JAMES W.
11018011	Not Issued	161	12/20/2004	Body biasing for dynamic circuit	TSCHANZ, JAMES W.
11018016	Not Issued	41	12/20/2004	Body biasing methods and circuits	TSCHANZ, JAMES W.
11038134	7164307	150	01/21/2005	BIAS GENERATOR FOR BODY BIAS	TSCHANZ, JAMES W.
11038394	Not Issued	95	01/21/2005	BIAS GENERATOR FOR BODY BIAS	TSCHANZ, JAMES W.
11053788	Not Issued	95	02/09/2005	MAJORITY VOTER CIRCUIT DESIGN	TSCHANZ, JAMES W.
11059174	Not Issued	30	02/16/2005	Representative majority voter for bus invert coding	TSCHANZ, JAMES W.
11094574	Not Issued	61	03/31/2005	Method and apparatus to adjust die frequency	TSCHANZ, JAMES W.
11134450	Not Issued	93	05/23/2005	REDUCING POWER CONSUMPTION IN INTEGRATED CIRCUITS	TSCHANZ, JAMES W.
11295400	Not Issued	30	12/06/2005	Component reliability budgeting system	TSCHANZ, JAMES W.
11314236	7190286	150	12/22/2005	SINGLE-STAGE AND MULTI-	TSCHANZ, JAMES

				STAGE LOW POWER INTERCONNECT ARCHITECTURES	W.
11320789	Not Issued	41	12/30/2005	Method and apparatus to clamp SRAM supply voltage	TSCHANZ, JAMES W.
11321100	Not Issued	25	12/29/2005	Reliability degradation compensation using body bias	TSCHANZ, JAMES W.
11324628	Not Issued	25	01/03/2006	Bidirectional body bias regulation	TSCHANZ, JAMES W.
11486030	Not Issued	30	07/14/2006	Method and apparatus for power consumption reduction	TSCHANZ, JAMES W.

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** tschanz **First Name** james Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page